LTC2420

20-Bit µPower No Latency ΔΣ™ ADC in SO-8

January 2000

FEATURES

- **20-Bit ADC in SO-8 Package**
- **8ppm INL, No Missing Codes at 20 Bits**
- **4ppm Full-Scale Error**
- **0.5ppm Offset**
- **1.2ppm Noise**
- **Digital Filter Settles in a Single Cycle. Each Conversion Is Accurate, Even After an Input Step.**
- Internal Oscillator—No External Components Required
- **Fast Mode: 16-Bit Noise, 12 Bits TUE at 100sps**
- 110dB Min, 50Hz/60Hz Notch Filter
- Reference Input Voltage: 0.1V to V_{CC}
- Live Zero—Extended Input Range Accommodates 12.5% Overrange and Underrange
- Single Supply 2.7V to 5.5V Operation
- Low Supply Current (200µA) and Auto Shutdown
- Pin Compatible with 24-Bit LTC2400

APPLICATIONS

- Weight Scales
- Direct Temperature Measurement
- Gas Analyzers
- Strain-Gage Transducers
- Instrumentation
- Data Acquisition
- Industrial Process Control
- 4-Digit DVMs

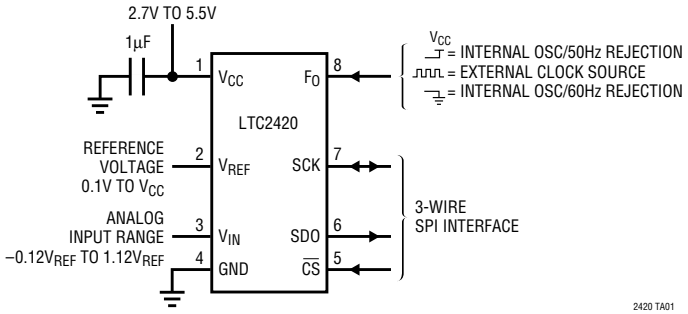
DESCRIPTION

The LTC®2420 is a micropower 20-bit A/D converter with an integrated oscillator, 8ppm INL and 1.2ppm RMS noise that operates from 2.7V to 5.5V. It uses delta-sigma technology and provides a digital filter that settles in a single cycle for multiplexed applications. Through a single pin, the LTC2420 can be configured for better than 110dB rejection at 50Hz or 60Hz ±2%, or it can be driven by an external oscillator for a user-defined rejection frequency in the range 1Hz to 800Hz. The internal oscillator requires no external frequency setting components.

The converter accepts any external reference voltage from 0.1V to V_{CC}. With its extended input conversion range of –12.5% V_{REF} to 112.5% V_{REF}, the LTC2420 smoothly resolves the offset and overrange problems of preceding sensors or signal conditioning circuits.

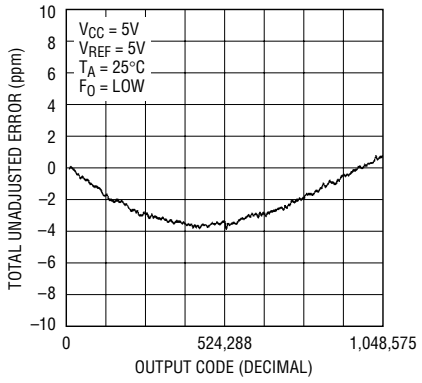
The LTC2420 communicates through a flexible 3-wire digital interface which is compatible with SPI and MICROWIRE™ protocols.

TYPICAL APPLICATION



2420 TA01

Total Unadjusted Error vs Output Code



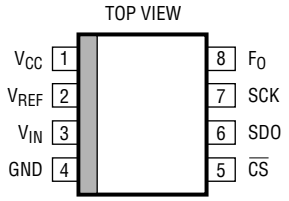
2420 TA02

ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{CC}) to GND .....–0.3V to 7V
Analog Input Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)
Reference Input Voltage to GND .. –0.3V to (V_{CC} + 0.3V)
Digital Input Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)
Digital Output Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)
Operating Temperature Range
LTC2420C ..... 0°C to 70°C
LTC2420I..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC2420CS8 LTC2420IS8
S8 PART MARKING
2420 2420I

Consult factory for Military grade parts.

CONVERTER CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 3, 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)	0.1V ≤ V_{REF} ≤ V_{CC}, (Note 5)	●	20			Bits
Integral Nonlinearity	V_{REF} = 2.5V (Note 6) V_{REF} = 5V (Note 6)	● ●		4 8	10 20	ppm of V_{REF} ppm of V_{REF}
Integral Nonlinearity (Fast Mode)	V_{REF} = 5V, V_{REF} = 2.5V, 100 Samples/Second, f_O = 2.048MHz	●		40	250	ppm of V_{REF}
Offset Error	2.5V ≤ V_{REF} ≤ V_{CC}	●		0.5	10	ppm of V_{REF}
Offset Error (Fast Mode)	2.5V < V_{REF} < 5V, 100 Samples/Second, f_O = 2.048MHz			3		ppm of V_{REF}
Offset Error Drift	2.5V ≤ V_{REF} ≤ V_{CC}			0.04		ppm of V_{REF}/°C
Full-Scale Error	2.5V ≤ V_{REF} ≤ V_{CC}	●		4	10	ppm of V_{REF}
Full-Scale Error (Fast Mode)	2.5V < V_{REF} < 5V, 100 Samples/Second, f_O = 2.048MHz			10		ppm of V_{REF}
Full-Scale Error Drift	2.5V ≤ V_{REF} ≤ V_{CC}			0.04		ppm of V_{REF}/°C
Total Unadjusted Error	V_{REF} = 2.5V V_{REF} = 5V			8 16		ppm of V_{REF} ppm of V_{REF}
Output Noise	V_{IN} = 0V (Note 13)			6		μV_{RMS}
Output Noise (Fast Mode)	V_{REF} = 5V, 100 Samples/Second, f_O = 2.048MHz			20		μV_{RMS}
Normal Mode Rejection 60Hz ±2%	(Note 7)	●	110	130		dB
Normal Mode Rejection 50Hz ±2%	(Note 8)	●	110	130		dB
Power Supply Rejection, DC	V_{REF} = 2.5V, V_{IN} = 0V			100		dB
Power Supply Rejection, 60Hz ±2%	V_{REF} = 2.5V, V_{IN} = 0V, (Note 7)			110		dB
Power Supply Rejection, 50Hz ±2%	V_{REF} = 2.5V, V_{IN} = 0V, (Note 8)			110		dB

ANALOG INPUT AND REFERENCE

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Voltage Range	(Note 14)	●	$-0.125 \cdot V_{REF}$		$1.125 \cdot V_{REF}$	V
V_{REF}	Reference Voltage Range		●	0.1		V_{CC}	V
$C_{S(IN)}$	Input Sampling Capacitance				1		pF
$C_{S(REF)}$	Reference Sampling Capacitance				1.5		pF
$I_{IN(LEAK)}$	Input Leakage Current	$\overline{CS} = V_{CC}$	●	–100	1	100	nA
$I_{REF(LEAK)}$	Reference Leakage Current	V_{REF} = 2.5V, $\overline{CS} = V_{CC}$	●	–100	1	100	nA

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage $\overline{CS}$, F_O	2.7V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 3.3V	●	2.5 2.0			V V
V_{IL}	Low Level Input Voltage $\overline{CS}$, F_O	4.5V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 5.5V	●			0.8 0.6	V V
V_{IH}	High Level Input Voltage SCK	2.7V ≤ V_{CC} ≤ 5.5V (Note 9) 2.7V ≤ V_{CC} ≤ 3.3V (Note 9)	●	2.5 2.0			V V
V_{IL}	Low Level Input Voltage SCK	4.5V ≤ V_{CC} ≤ 5.5V (Note 9) 2.7V ≤ V_{CC} ≤ 5.5V (Note 9)	●			0.8 0.6	V V
I_{IN}	Digital Input Current $\overline{CS}$, F_O	0V ≤ V_{IN} ≤ V_{CC}	●	–10		10	µA
I_{IN}	Digital Input Current SCK	0V ≤ V_{IN} ≤ V_{CC} (Note 9)	●	–10		10	µA
C_{IN}	Digital Input Capacitance $\overline{CS}$, F_O				10		pF
C_{IN}	Digital Input Capacitance SCK	(Note 9)			10		pF
V_{OH}	High Level Output Voltage SDO	I_O = –800µA	●	V_{CC} – 0.5			V
V_{OL}	Low Level Output Voltage SDO	I_O = 1.6mA	●			0.4	V
V_{OH}	High Level Output Voltage SCK	I_O = –800µA (Note 10)	●	V_{CC} – 0.5			V
V_{OL}	Low Level Output Voltage SCK	I_O = 1.6mA (Note 10)	●			0.4	V
I_{OZ}	High-Z Output Leakage SDO		●	–10		10	µA

POWER REQUIREMENTS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	2.7		5.5	V
I_{CC}	Supply Current Conversion Mode Sleep Mode	 $\overline{CS}$ = 0V (Note 12) $\overline{CS} = V_{CC}$ (Note 12)	 ● ●		 200 20	 300 30	 µA µA

TIMING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range	20-Bit Effective Resolution 12-Bit Effective Resolution	● ●	2.56 2.56		307.2 2.048	kHz MHz
t_{HEO}	External Oscillator High Period		●	0.5		390	µs
t_{LEO}	External Oscillator Low Period		●	0.5		390	µs
t_{CONV}	Conversion Time	F_O = 0V F_O = V_{CC} External Oscillator (Note 11)	● ● ●	130.66 156.80 20480/f_{EOSC} (in kHz)	133.33 160	136 163.20	ms ms ms
f_{ISCK}	Internal SCK Frequency	Internal Oscillator (Note 10) External Oscillator (Notes 10, 11)		19.2 f_{EOSC}/8			kHz kHz
D_{ISCK}	Internal SCK Duty Cycle	(Note 10)		45		55	%
f_{ESCK}	External SCK Frequency Range	(Note 9)	●			2000	kHz
t_{LESCK}	External SCK Low Period	(Note 9)	●	250			ns
t_{HESCK}	External SCK High Period	(Note 9)	●	250			ns
t_{DOUT_ISCK}	Internal SCK 24-Bit Data Output Time	Internal Oscillator (Notes 10, 12) External Oscillator (Notes 10, 11)	● ●	1.23 192/f_{EOSC} (in kHz)	1.25	1.28	ms ms
t_{DOUT_ESCK}	External SCK 24-Bit Data Output Time	(Note 9)	●	24/f_{ESCK} (in kHz)			ms
t_1	$\overline{CS}$ ↓ to SDO Low Z		●	0		150	ns
t2	$\overline{CS}$ ↑ to SDO High Z		●	0		150	ns
t3	$\overline{CS}$ ↓ to SCK ↓	(Note 10)	●	0		150	ns
t4	$\overline{CS}$ ↓ to SCK ↑	(Note 9)	●	50			ns
t_{KQMAX}	SCK ↓ to SDO Valid		●			200	ns
t_{KQMIN}	SDO Hold After SCK ↓	(Note 5)	●	15			ns
t_5	SCK Set-Up Before $\overline{CS}$ ↓		●	50			ns
t_6	SCK Hold After $\overline{CS}$ ↓		●			50	ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: All voltages are with respect to GND. V_{CC} = 2.7 to 5.5V unless otherwise specified. R_{SOURCE} = 0Ω.

Note 4: Internal Conversion Clock source with the F_O pin tied to GND or to V_{CC} or to external conversion clock source with f_{EOSC} = 153600Hz unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: F_O = 0V (internal oscillator) or f_{EOSC} = 153600Hz ±2% (external oscillator).

Note 8: F_O = V_{CC} (internal oscillator) or f_{EOSC} = 128000Hz ±2% (external oscillator).

Note 9: The converter is in external SCK mode of operation such that the SCK pin is used as digital input. The frequency of the clock signal driving SCK during the data output is f_{ESCK} and is expressed in kHz.

Note 10: The converter is in internal SCK mode of operation such that the SCK pin is used as digital output. In this mode of operation the SCK pin has a total equivalent load capacitance C_{LOAD} = 20pF.

Note 11: The external oscillator is connected to the F_O pin. The external oscillator frequency, f_{EOSC}, is expressed in kHz.

Note 12: The converter uses the internal oscillator. F_O = 0V or F_O = V_{CC}.

Note 13: The output noise includes the contribution of the internal calibration operations.

Note 14: For reference voltage values V_{REF} > 2.5V the extended input of –0.125 • V_{REF} to 1.125 • V_{REF} is limited by the absolute maximum rating of the Analog Input Voltage pin (Pin 3). For 2.5V < V_{REF} ≤ 0.267V + 0.89 • V_{CC} the input voltage range is –0.3V to 1.125 • V_{REF}. For 0.267V + 0.89 • V_{CC} < V_{REF} ≤ V_{CC} the input voltage range is –0.3V to V_{CC} + 0.3V.

PIN FUNCTIONS

V_{CC} (Pin 1): Positive Supply Voltage. Bypass to GND (Pin 4) with a 10µF tantalum capacitor in parallel with 0.1µF ceramic capacitor as close to the part as possible.

V_{REF} (Pin 2): Reference Input. The reference voltage range is 0.1V to V_{CC}.

V_{IN} (Pin 3): Analog Input. The input voltage range is $-0.125 \cdot V_{REF}$ to $1.125 \cdot V_{REF}$. For $V_{REF} > 2.5V$ the input voltage range may be limited by the pin absolute maximum rating of –0.3V to V_{CC} + 0.3V.

GND (Pin 4): Ground. Shared pin for analog ground, digital ground, reference ground and signal ground. Should be connected directly to a ground plane through a minimum length trace or it should be the single-point-ground in a single point grounding system.

$\overline{CS}$ (Pin 5): Active LOW Digital Input. A LOW on this pin enables the SDO digital output and wakes up the ADC. Following each conversion, the ADC automatically enters the Sleep mode and remains in this low power state as long as $\overline{CS}$ is HIGH. A LOW on $\overline{CS}$ wakes up the ADC. A LOW-to-HIGH transition on this pin disables the SDO digital output. A LOW-to-HIGH transition on $\overline{CS}$ during the Data Output transfer aborts the data transfer and starts a new conversion.

SDO (Pin 6): Three-State Digital Output. During the data output period this pin is used for serial data output. When the chip select $\overline{CS}$ is HIGH ($\overline{CS} = V_{CC}$), the SDO pin is in a high impedance state. During the Conversion and Sleep periods, this pin can be used as a conversion status output. The conversion status can be observed by pulling $\overline{CS}$ LOW.

SCK (Pin 7): Bidirectional Digital Clock Pin. In Internal Serial Clock Operation mode, SCK is used as digital output for the internal serial interface clock during the data output period. In External Serial Clock Operation mode, SCK is used as digital input for the external serial interface. A weak internal pull-up is automatically activated in Internal Serial Clock Operation mode. The Serial Clock mode is determined by the level applied to SCK at power up and the falling edge of $\overline{CS}$.

F_O (Pin 8): Frequency Control Pin. Digital input that controls the ADC's notch frequencies and conversion time. When the F_O pin is connected to V_{CC} ($F_O = V_{CC}$), the converter uses its internal oscillator and the digital filter's first null is located at 50Hz. When the F_O pin is connected to GND (F_O = 0V) the converter uses its internal oscillator and the digital filter first null is located at 60Hz. When F_O is driven by an external clock signal with a frequency f_{EOSC}, the converter uses this signal as its clock and the digital filter first null is located at a frequency $f_{EOSC}/2560$.

APPLICATIONS INFORMATION

The LTC2420 is pin compatible with the LTC2400. The two devices are designed to allow the user to incorporate either device in the same design with no modifications. While the LTC2420 output word length is 24 bits (as opposed to the 32-bit output of the LTC2400), its output clock timing can be identical to the LTC2400. As shown in Figure 1, the LTC2420 data output is concluded on the falling edge of the 24th serial clock (SCK). In order to maintain drop-in compatibility with the LTC2400, it is possible to clock the LTC2420 with an additional 8 serial clock pulses. This results in 8 additional output bits which are always logic HIGH.

Output Data Format

The LTC2420 serial output data stream is 24 bits long. The first 4 bits represent status information indicating the sign, input range and conversion state. The next 20 bits are the conversion result, MSB first.

Bit 23 (first output bit) is the end of conversion ($\overline{EOC}$) indicator. This bit is available at the SDO pin during the conversion and sleep states whenever the $\overline{CS}$ pin is LOW. This bit is HIGH during the conversion and goes LOW when the conversion is complete.

Bit 22 (second output bit) is a dummy bit (DMY) and is always LOW.

APPLICATIONS INFORMATION

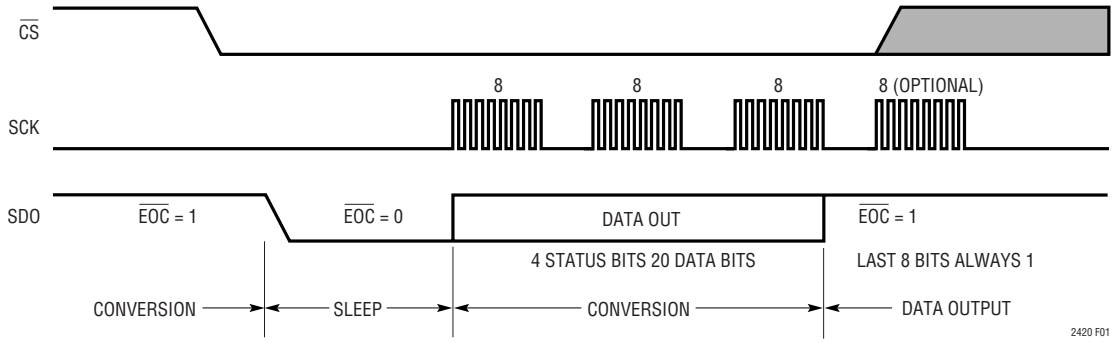


Figure 1. LTC2420 Compatible Timing with the LTC2400

Bit 21 (third output bit) is the conversion result sign indicator (SIG). If V_{IN} is >0, this bit is HIGH. If V_{IN} is <0, this bit is LOW. The sign bit changes state during the zero code.

Bit 20 (forth output bit) is the extended input range (EXR) indicator. If the input is within the normal input range $0 \le V_{IN} \le V_{REF}$, this bit is LOW. If the input is outside the normal input range, $V_{IN} > V_{REF}$ or $V_{IN} < 0$, this bit is HIGH.

The function of these bits is summarized in Table 1.

Table 1. LTC2420 Status Bits

Input Range	Bit 23 $\overline{EOC}$	Bit 22 DMY	Bit 21 SIG	Bit 20 EXR
$V_{IN} > V_{REF}$	0	0	1	1
$0 < V_{IN} \le V_{REF}$	0	0	1	0
$V_{IN} = 0^+/0^-$	0	0	1/0	0
$V_{IN} < 0$	0	0	0	1

Bit 19 (fifth output bit) is the most significant bit (MSB).

Bits 19-0 are the 20-bit conversion result MSB first.

Bit 0 is the least significant bit (LSB).

Data is shifted out of the SDO pin under control of the serial clock (SCK), see Figure 2. Whenever $\overline{CS}$ is HIGH, SDO remains high impedance and any SCK clock pulses are ignored by the internal data out shift register.

In order to shift the conversion result out of the device, $\overline{CS}$ must first be driven LOW. $\overline{EOC}$ is seen at the SDO pin of the device once $\overline{CS}$ is pulled LOW. $\overline{EOC}$ changes real time from HIGH to LOW at the completion of a conversion. This signal may be used as an interrupt for an external microcontroller. Bit 23 ($\overline{EOC}$) can be captured on the first rising edge of SCK. Bit 22 is shifted out of the device on the first falling edge of SCK. The final data bit (Bit 0) is shifted out on the falling edge of the 23rd SCK and may be latched on the rising edge of the 24th SCK pulse. On the falling edge of the 24th SCK pulse, SDO goes HIGH indicating a new conversion cycle has been initiated. This bit serves as $\overline{EOC}$ (Bit 23) for the next conversion cycle. Table 2 summarizes the output data format.

As long as the voltage on the V_{IN} pin is maintained within the –0.3V to (V_{CC} + 0.3V) absolute maximum operating range, a conversion result is generated for any input value from $-0.125 \cdot V_{REF}$ to $1.125 \cdot V_{REF}$. For input voltages greater than $1.125 \cdot V_{REF}$, the conversion result is clamped to the value corresponding to $1.125 \cdot V_{REF}$. For input voltages below $-0.125 \cdot V_{REF}$, the conversion result is clamped to the value corresponding to $-0.125 \cdot V_{REF}$.

Operation at Higher Data Output Rates

The LTC2420 typically operates with an internal oscillator of 153.6kHz. This corresponds to a notch frequency of 60Hz and an output rate of 7.5 samples/second. The internal oscillator is enabled if the F_O pin is logic LOW (logic HIGH for a 50Hz notch). It is possible to drive the F_O pin with an external oscillator for higher data output rates. As shown in Figure 3, an external clock of 2.048MHz applied to the F_O pin results in a notch frequency of 800Hz with a data output rate of 100 samples/second.

Figure 4 shows the total unadjusted error (Offset Error + Full-Scale Error + INL + DNL) as a function of the output data rate with a 5V reference. The relationship between the

APPLICATIONS INFORMATION

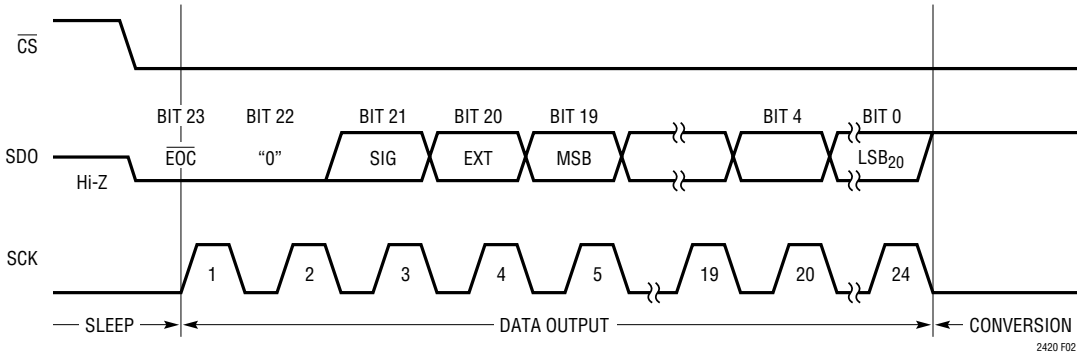


Figure 2. Output Data Timing

Table 2. LTC2420 Output Data Format

Input Voltage	Bit 23 $\overline{EOC}$	Bit 22 DMY	Bit 21 SIG	Bit 20 EXR	Bit 19 MSB	Bit 18	Bit 17	Bit 16	Bit 15	…	Bit 0 LSB
$V_{IN} > 9/8 \cdot V_{REF}$	0	0	1	1	0	0	0	1	1	...	1
$9/8 \cdot V_{REF}$	0	0	1	1	0	0	0	1	1	...	1
V_{REF} + 1LSB	0	0	1	1	0	0	0	0	0	...	0
V_{REF}	0	0	1	0	1	1	1	1	1	...	1
$3/4V_{REF}$ + 1LSB	0	0	1	0	1	1	0	0	0	...	0
$3/4V_{REF}$	0	0	1	0	1	0	1	1	1	...	1
$1/2V_{REF}$ + 1LSB	0	0	1	0	1	0	0	0	0	...	0
$1/2V_{REF}$	0	0	1	0	0	1	1	1	1	...	1
$1/4V_{REF}$ + 1LSB	0	0	1	0	0	1	0	0	0	...	0
$1/4V_{REF}$	0	0	1	0	0	0	1	1	1	...	1
$0^+/0^-$	0	0	1/0*	0	0	0	0	0	0	...	0
–1LSB	0	0	0	1	1	1	1	1	1	...	1
$-1/8 \cdot V_{REF}$	0	0	0	1	1	1	1	0	0	...	0
$V_{IN} < -1/8 \cdot V_{REF}$	0	0	0	1	1	1	1	0	0	...	0

*The sign bit changes state during the 0 code.

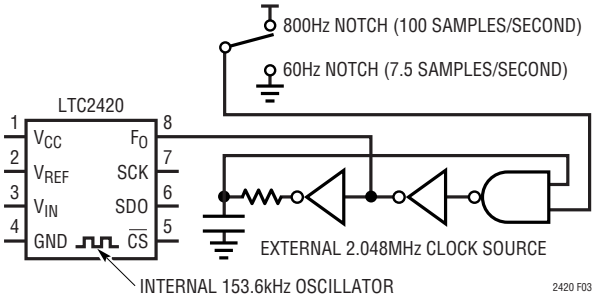


Figure 3. Selectable 100 Samples/Second Turbo Mode

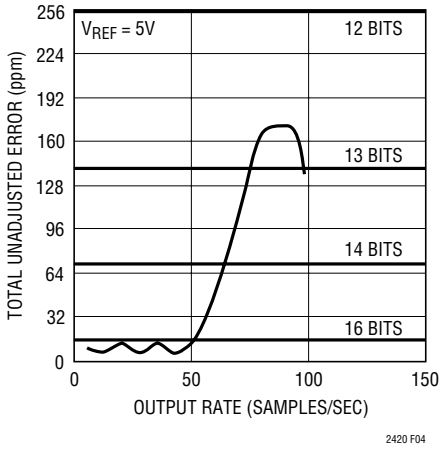


Figure 4. Total Error vs Output Rate (V_{REF} = 5V)

APPLICATIONS INFORMATION

output data rate (ODR) and the frequency applied to the F_O pin (F_O) is:

$$ODR = F_O/20480$$

For output data rates up to 50 samples/second, the total unadjusted error (TUE) is better than 16 bits, and better than 12 bits at 100 samples/second. As shown in Figure 5, for output data rates of 100 samples/second, the TUE is better than 15 bits for V_{REF} below 2.5V. Figure 6 shows an unaveraged total unadjusted error for the LTC2420 operating at 100 samples/second with V_{REF} = 2.5V. Figure 7 shows the same device operating with a 5V reference and an output data rate of 7.5 samples/second.

At 100 samples/second, the LTC2420 can be used to capture transient data. This is useful for monitoring settling or auto gain ranging in a system. The LTC2420 can monitor signals at an output rate of 100 samples/second. After acquiring 100 samples/second data the F_O pin may be driven LOW enabling 60Hz rejection to 110dB and the highest possible DC accuracy. The no latency architecture of the LTC2420 allows consecutive readings (one at 100 samples/second the next at 7.5 samples/second) without interaction between the two readings.

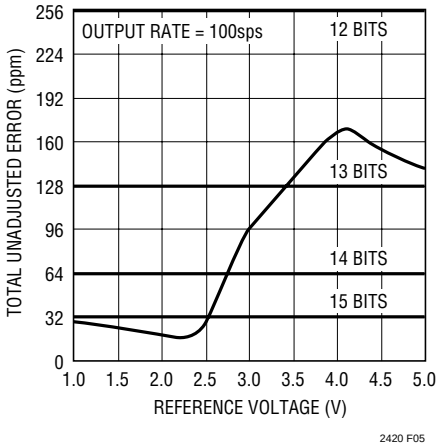


Figure 5. Total Error vs V_{REF} (Output Rate = 100sps)

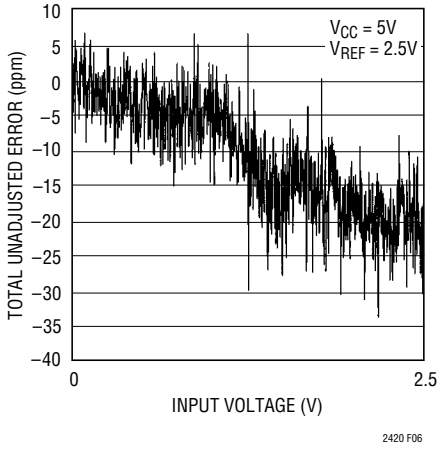


Figure 6. Total Unadjusted Error at 100 Samples/Second (No Averaging)

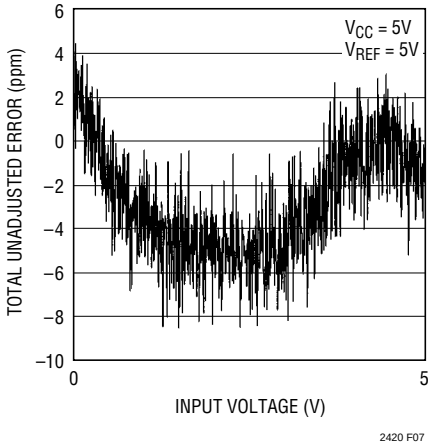
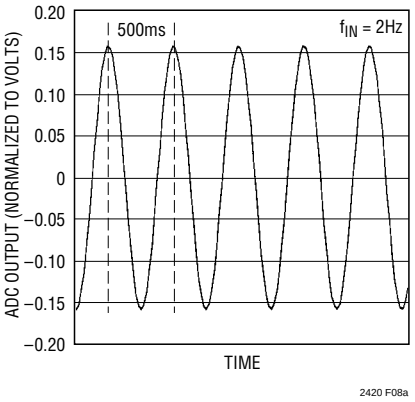


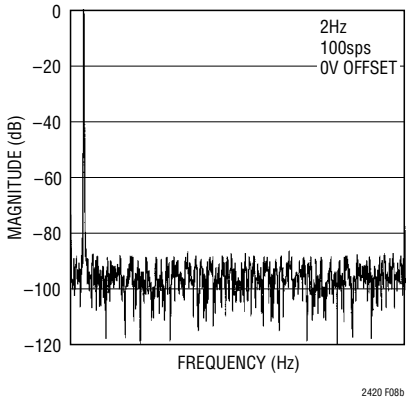
Figure 7. Total Unadjusted Error at 7.5 Samples/Second (No Averaging)

APPLICATIONS INFORMATION

As shown in Figure 8, the LTC2420 can capture transient data with 90dB of dynamic range (with a 300mV$_{P-P}$ input signal at 2Hz). The exceptional DC performance of the LTC2420 enables signals to be digitized independent of a large DC offset. Figures 9a and 9b show the dynamic performance with a 15Hz signal superimposed on a 2V DC level. The same signal with no DC level is shown in Figures 9c and 9d.

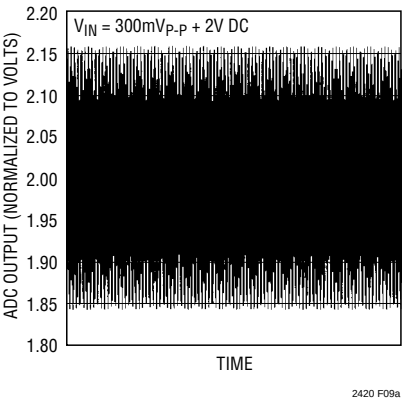


8a. Digitized Waveform

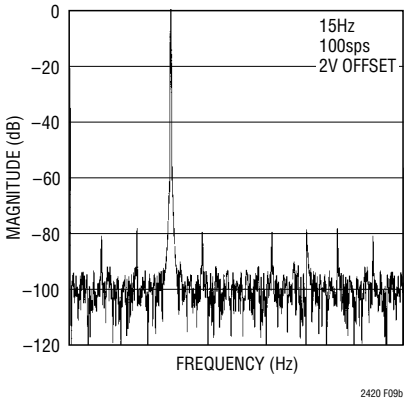


8b. Output FFT

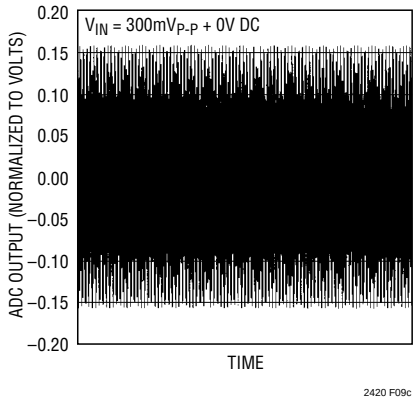
Figure 8. Transient Signal Acquisiton



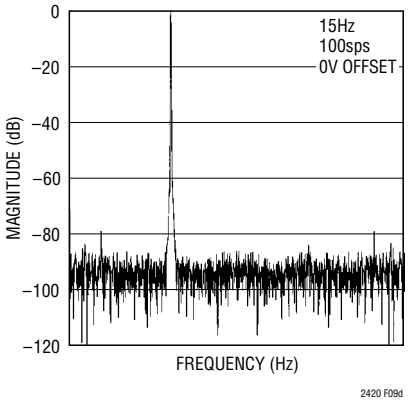
9a. Digitized Waveform with 2V DC Offset



9b. FFT Waveform with 2V DC Offset



9c. Digitized Waveform with No Offset



9d. FFT Waveform with No Offset

Figure 9. Using the LTC2420's High Accuracy Wide Dynamic Range to Digitize a 300mV$_{P-P}$ 15Hz Waveform with a Large DC Offset (V_{CC} = 5V, V_{REF} = 5V)

APPLICATIONS INFORMATION

Single-Chip Instrumentation Amplifier for the LTC2420

The circuit in Figure 10 is a simple solution for processing differential signals in pressure transducer, weigh scale or strain gauge applications that can operate on a supply voltage range of ±5V to ±15V. The circuit uses an LT®1920 single-chip instrumentation amplifier to perform a differential to single-ended conversion. The amplifier's output voltage is applied to the LTC2420's input and converted to a digital value with an overall accuracy exceeding 17 bits (0.0008%). Key circuit performance results are shown in Table 3.

The practical gain range for this topology as shown is from 5 to 100 because the LTC2420's wide dynamic range makes gains below 5 virtually unnecessary, whereas gain up to 100 significantly reduce the input referred noise.

The optional passive RC lowpass filter between the amplifier's output and the LTC2420's input attenuates high frequency noise and its effects. Typically, the filter reduces the magnitude of averaged noise by 30% and improves resolution by 0.5 bit without compromising linearity. Resistor R2 performs two functions: it isolates C1 from the LTC2420's input and limits the LTC2420's input current should its input voltage drop below –300mV or swing above V_{CC} + 300mV.

The LT1920 is the choice for applications where low cost is important. For applications where more precision is required, the LT1167 is a pin-to-pin alternative choice with a lower offset voltage, lower input bias current and higher gain accuracy than the LT1920. The LT1920's maximum total input-referred offset (V_{OST}) is 135μV for a gain of 100. At the same gain, the LT1167's V_{OST} is 63μV. At gains of 10 or 100, the LT1920's maximum gain error is 0.3% and its maximum gain nonlinearity is 30ppm. At the same gains, the LT1167's maximum gain error is 0.1% and its maximum gain nonlinearity is 15ppm. Table 4 summarizes the performance of Figure 10's circuit using the LT1167.

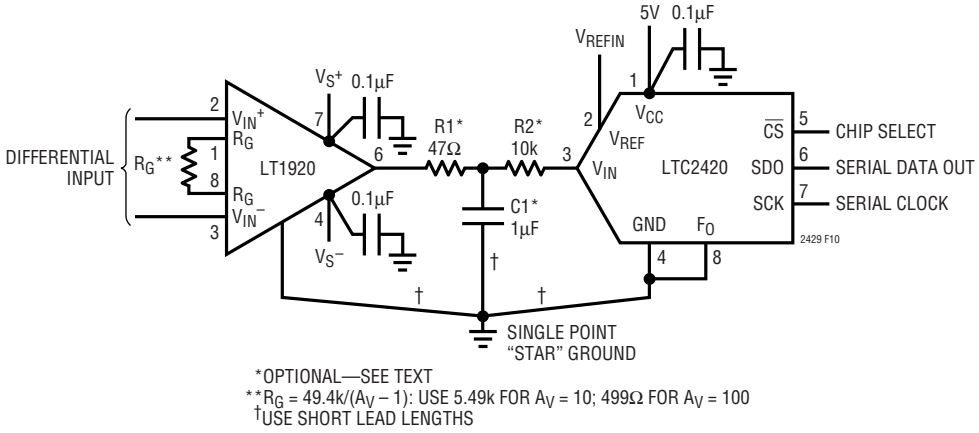


Figure 10. The LT1920 is a Simple Solution That Converts a Differential Input to a Ground Referred Single-Ended Signal for the LTC2420

APPLICATIONS INFORMATION

Table 3. Typical Performance of the LTC2420 ADC When Used with the LT1920 Instrumentation Amplifiers in Figure 9's Differential Digitizing Circuit

	V_S = ±5V		V_S = ±15V		
PARAMETER	A_V = 10	A_V = 100	A_V = 10	A_V = 100	TOTAL (UNITS)
Differential Input Voltage Range	–30 to 400	–3 to 40	–30 to 500	–3 to 50	mV
Zero Error	–160	–2650	–213	–2625	µV
Maximum Input Current		2.0			nA
Nonlinearity	±8.2	±7.4	±6.5	±6.1	ppm
Noise (Without Averaging)	1.8*	0.25*	1.5*	0.27*	μV_{RMS}
Noise (Averaged 64 Readings)	0.2*	0.03*	0.19*	0.03*	μV_{RMS}
Resolution (with Averaged Readings)	21	20.6	21.3	20.5	Bits
Overall Accuracy (Uncalibrated)	17.2	17.3	17.5	18.2	Bits
Common Mode Rejection Ratio		≥120			dB
Common Mode Range	2/–1.5**	2.2/–1.7**	11.5/–11**	11.7/–11.2**	V

*Input referred noise for the respective gain. **Typical values based on single lab tested sample of each amplifier.

Table 4. Typical Performance of the LTC2420 ADC When Used with the LT1167 Instrumentation Amplifiers in Figure 9's Differential Digitizing Circuit

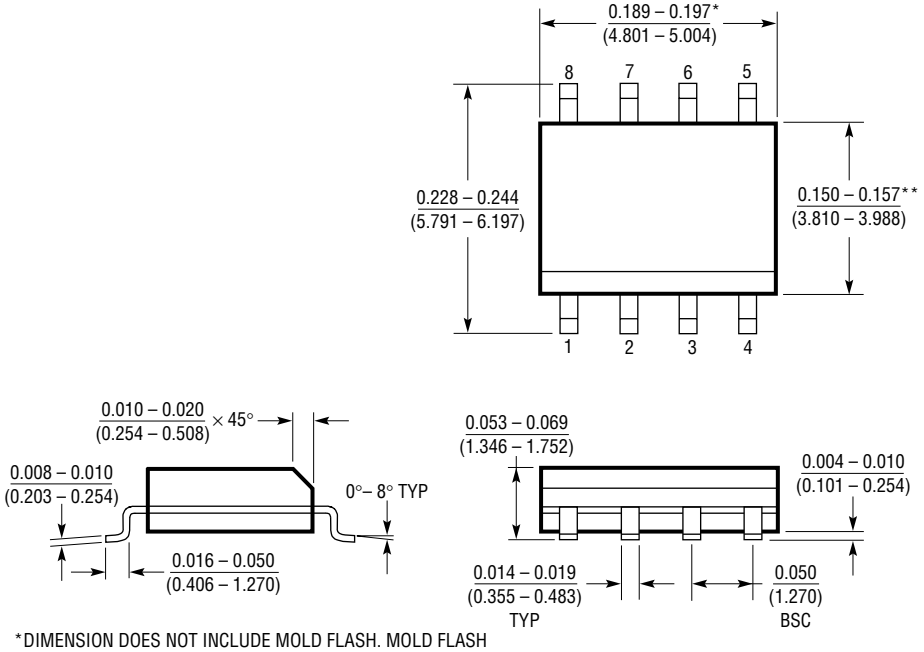
	V_S = ±5V		V_S = ±15V		
PARAMETER	A_V = 10	A_V = 100	A_V = 10	A_V = 100	TOTAL (UNITS)
Differential Input Voltage Range	–30 to 400	–3 to 40	–30 to 500	–3 to 50	mV
Zero Error	–94	–1590	–110	–1470	µV
Maximum Input Current		0.5			nA
Nonlinearity	±4.1	±4.4	±4.1	±3.7	ppm
Noise (Without Averaging)	1.4*	0.19*	1.5*	0.18*	μV_{RMS}
Noise (Averaged 64 Readings)	0.18*	0.02*	0.19*	0.02*	μV_{RMS}
Resolution (with Averaged Readings)	21.4	21.0	21.3	21.1	Bits
Overall Accuracy (Uncalibrated)	18.2	18.1	18.2	19.4	Bits
Common Mode Rejection Ratio		≥120			dB
Common Mode Range	2/–1.5**	2.2/–1.7**	11.5/–11**	11.7/–11.2**	V

*Input referred noise for the respective gain. **Typical values based on single lab tested sample of each amplifier.

PACKAGE INFORMATION

Dimensions in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

SO8 1298

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1019	Precision Bandgap Reference, 2.5V, 5V	3ppm/°C Drift, 0.05% Max
LT1025	Micropower Thermocouple Cold Junction Compensator	0.5°C Initial Accuracy, 80μA Supply Current
LTC1043	Dual Precision Instrumentation Switched Capacitor Building Block	Precise Charge, Balanced Switching, Low Power
LTC1050	Precision Chopper Stabilized Op Amp	No External Components 5μV Offset, 1.6μV_{P-P} Noise
LT1236A-5	Precision Bandgap Reference, 5V	0.05% Max, 5ppm/°C Drift
LTC1391	8-Channel Multiplexer	Low R_{ON}: 45Ω, Low Charge Injection, Serial Interface
LT1460	Micropower Series Reference	0.075% Max, 10ppm/°C Max Drift, 2.5V, 5V and 10V Versions, MSOP, PDIP, SO-8, SOT-23 and TO-92 Packages
LTC2400	24-Bit μPower, No Latency ΔΣ ADC in SO-8	4ppm INL, 10ppm Total Unadjusted Error, 200μA
LTC2408	8-Channel, 24-Bit No Latency ΔΣ ADC	4ppm INL, 10ppm Total Unadjusted Error, 200μA

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408)432-1900 • FAX: (408) 434-0507 • www.linear-tech.com
2420i LT/TP 0100 4K • PRINTED IN USA